I Claim:

1. In a memory cell array having word lines, bit lines organized in pairs, and memory cells addressable via the word lines and the bit lines, each of the memory cells having a respective storage capacitor, and each of the storage capacitors being connectable to one of the bit lines of one of the bit line pairs by activation by one of the word lines; a read-out circuit, comprising:

an interchanging circuit connected to each of the bit lines of one of the bit line pairs and having a first data output line, a second data output line adjacent said first data output line, a third data output line adjacent said second output line, and a fourth data output line adjacent said third output line;

said interchanging circuit being configured to apply the bit lines connected to the storage capacitors to said second and third data output lines by activating the word line and to apply the bit lines not connected to the memory cells to said first and fourth data output lines;

a first sense amplifier connected to said first and second data output lines;

a second sense amplifier connected to said third and fourth data output lines; and

a third sense amplifier connected to said second and third data output lines;

said first, second, and third sense amplifiers each being configured to amplify a potential difference on said respective two connected lines.

2. The read-out circuit according to claim 1, wherein:

a first and a second word line are provided;

the first bit line of the respective bit line pair is configured to be connected to the corresponding storage capacitors by activating the first word line and the second bit line of the respective bit line pair being configured to connect to the corresponding storage capacitors by activating the second word line;

said interchanging circuit being configured to apply, when activating the first word line, the first bit lines of the two bit line pairs to said second and said third data output line and sad second bit lines to said first and said fourth data output line, and to apply, when activating the second word

line, the second bit lines of the two bit line pairs to said second and said third data output line and the first bit lines to said first and said fourth data output line.

3. The read-out circuit according to claim 1, further comprising a first and second bit line potential;

said sense amplifiers each having respective a first transistor, a second transistor, a third transistor, and a fourth transistor;

a first terminal of said first transistor being connected to the first bit line and a second terminal of said first transistor being connected to said first bit line potential;

a first terminal of said second transistor being connected to the second bit line and a second terminal of said second transistor being connected to said first bit line potential;

a first terminal of said third transistor being connected to the first bit line and a second terminal of said third transistor being connected to said second bit line potential; and

a first terminal of said fourth transistor being connected to the second bit line and a second terminal of said fourth transistor being connected to said second bit line potential.

4. The read-out circuit according to claim 1, wherein:

said first, second, and third sense amplifiers have respective driver strengths; and

the driver strength of said third sense amplifier is less than at least one of the driver strength of said first and said second sense amplifiers.

5. The read-out circuit according to claim 1, further comprising a potential equalization circuit disposed between said first data output line and said fourth data output line and configured to equalize potentials between said first data output line and said fourth data output line depending on an equalization control signal.

6. A memory cell array, comprising:

word lines;

bit lines organized in pairs;

memory cells addressable via said word lines and said bit lines, each of said memory cells having a respective storage capacitor, and each of said storage capacitors being connectable to one of said bit lines of one of said bit line pairs by activation by one of said word lines; and

a read-out circuit including:

an interchanging circuit connected to each of said bit lines of one of said bit line pairs and having a first data output line, a second data output line adjacent said first data output line, a third data output line adjacent said second output line, and a fourth data output line (DQ2C) adjacent said third output line;

said interchanging circuit being configured to apply said bit lines connected to said storage capacitors to said second and third data output lines by activating said word line and to apply said bit lines not connected to the memory cells to said first and fourth data output lines;

a first sense amplifier connected to said first and second data output lines;

a second sense amplifier connected to said third and fourth data output lines; and

a third sense amplifier connected to said second and third data output lines;

said first, second, and third sense amplifiers each being configured to amplify a potential difference on said respective two connected lines.

7. A method for amplifying and reading data stored in a memory cell array, which comprises:

providing a read-out circuit according to claim 1;

activating one of the word lines; and

driving the interchanging circuit to apply the bit lines connected to the storage capacitors to the second and third data output lines.

8. The method according to claim 7, which further comprises applying an nset signal and a pset signal to the first and second sense amplifiers simultaneously with the activating of the word line, the nset signal and the pset signal determining a high and a low potential for the data output lines.

9. The method according to claim 8, which further comprises applying an npuls signal and a ppuls signal, to the third sense amplifier simultaneously with the activating of the word line, the npuls signal and the ppuls signal being pulsed with respect to the nset signal and a pset signal, the npuls signal and the ppuls signal determining a high and a low potential for the data output lines.